1 MSPS, 12 Bit Single-Ended Analog-to-Digital Converter

1 FEATURES

- **Variable Power Management**
- **Packaged in SOT23-6**
- **Power Supply Used as Reference**
- **Single 2.7V to 5.25V Supply Operation**
- **Compatible With SPI™, QSPI™, MICROWIRE™, and DSP**
- **Key Specifications**
  - **Resolution with No Missing Codes**
  - **Conversion Rate: 1 MSPS**
  - **DNL: 0.6, -0.3 LSB (Typical)**
  - **INL: ±0.6 LSB (Typical)**
  - **Power Consumption:**
    - **3V Supply: 4.5mW (Typical)**
    - **5V Supply: 11mW (Typical)**

2 APPLICATIONS

- **Automotive Navigation**
- **FA or ATM Equipment**
- **Portable Systems**
- **Medical Instruments**
- **Mobile Communications**
- **Instrumentation and Control Systems**

3 DESCRIPTIONS

The RS1461 is a low power, monolithic CMOS 12-bit analog-to-digital converter that operates at 1 MSPS. The RS1461 is a drop-in replacement for Texas Instruments' ADCS7476. This device is based on a successive approximation register architecture with internal track-and-hold. The serial interface is compatible with several standards, such as SPI, QSPI, MICROWIRE, and many common DSP serial interfaces.

The RS1461 uses the supply voltage as a reference, enabling the device to operate with a full-scale input range of 0 to V_{DD}. The conversion rate is determined from the serial clock (SCLK) speed. This converter offers a shutdown mode, which can be used to trade throughput for power consumption. The RS1461 is operated with a single supply that can range from 2.7V to 5.25V. Normal power consumption during continuous conversion, using a 3V or 5V supply, is 4.5mW or 11mW respectively. The power-down feature, which is enabled by a chip select ($\overline{CS}$) pin, reduces the power consumption to under 5µW using a 5V supply. This converter is available in a 6-pin SOT-23 package, which provides an extremely small footprint for applications where space is a critical consideration. This product is designed for operation over the automotive and extended industrial temperature range of -40°C to 125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS1461	SOT23-6	2.92mm×1.60mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

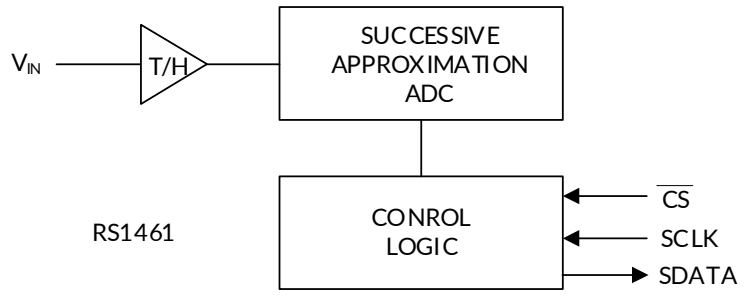


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4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2023/06/19	Preliminary version completed
A.1	2023/11/21	Initial version completed
A.2	2025/10/15	Update PACKAGE OUTLINE DIMENSIONS

5 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL(3)	PACKAGE OPTION
RS1461	RS1461XH	-40°C ~+125°C	SOT23-6	1461	MSL1	Tape and Reel,3000

NOTE:

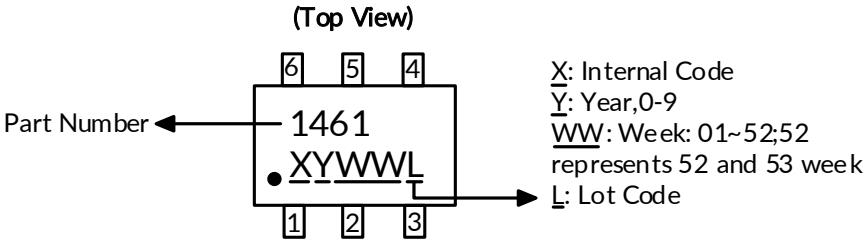
(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information(data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F, Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

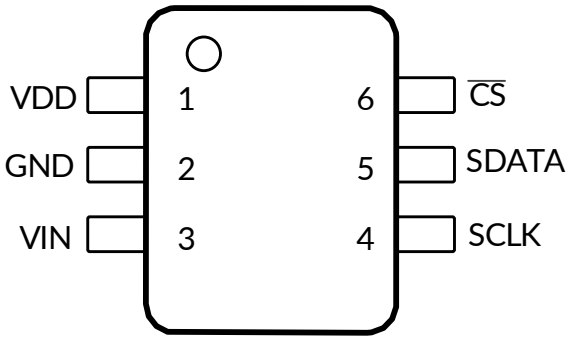
Marking Information

(1) SOT23-6



6 PIN CONFIGURATION AND FUNCTIONS (TOP VIEW)

Top View



SOT23-6

Pin Description

NAME	PIN	I/O (1)	DESCRIPTION
	SOT23-6		
VDD	1	P	Positive supply pin. These pins must be connected to a quiet 2.7V to 5.25V source and bypassed to GND with 0.1μF and 1μF monolithic capacitors placed within 1 cm of the power pin. RS1461 uses this power supply as a reference, so it must be thoroughly bypassed.
GND	2	G	The ground return for the supply.
VIN	3	I	Analog input. This signal can range from 0 V to VDD.
SCLK	4	I	Digital clock input. The range of frequencies for this input is 10 kHz to 20 MHz, with ensured performance at 20MHz. This clock directly controls the conversion and readout processes.
SDATA	5	O	Digital data output. The output words are clocked out of this pin by the SCLK pin.
$\overline{CS}$	6	I	Chip select. A conversion process begins on the falling edge of $\overline{CS}$.

(1) G = Ground, I = Input, O = Output, P = Power

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Supply voltage, V_{DD}			-0.3	6.5	V
Voltage on any analog pin to GND			-0.3	V_{DD}+0.3	V
Voltage on any digital pin to GND			-0.3	6.5	V
Input current at any pin (except power supply pins)				±10	mA
θ_{JA}	Package thermal impedance (4)	SOT23-6		230	°C/W
Soldering temperature, infrared (10 sec)				215	°C
Operating temperature,T_A				150	°C
Storage temperature, T_{stg}			-65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Analog input terminal is diode-clamped to the power-supply rails. Input signal that can swing more than 0.3V beyond the supply rails should be current-limited to 10mA or less.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.
(4) The package thermal impedance is calculated in accordance with JESD-51.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	
		Machine Model (MM)	±150	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.



ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	2.7		5.25	V
	Digital input pins voltage (independent of supply voltage)	2.7		5.25	
T_A	Operating temperature	-40		125	°C

7.4 Electrical Characteristics

T_A = 25°C, V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, and f_{SAMPLE} = 1 MSPS (unless otherwise noted) (1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CONVERTER CHARACTERISTICS						
	Resolution with no missing codes	-40°C ≤T_A ≤ 125°C			12	Bits
INL	Integral non-linearity	-40°C ≤T_A ≤ 125°C	-1	±0.6	+1	LSB
DNL	Differential non-linearity	-40°C ≤T_A ≤ 125°C	-0.8	0.6/-0.3	+1	LSB
V_{OFF}	Offset error	-40°C ≤T_A ≤ 125°C	-2	±1.2	+2	LSB
GE	Gain error	-40°C ≤T_A ≤ 125°C	-1.2	±0.6	+1.2	LSB
TUE	Total Unadjusted Error	-40°C ≤T_A ≤ 125°C		±1.2		LSB
DYNAMIC CONVERTER CHARACTERISTICS						
SINAD	Signal-to-noise plus distortion ratio	f_{IN}=100kHz, -40°C ≤T_A ≤ 125°C	70	71.5		dB
SNR	Signal-to-noise ratio	f_{IN}=100kHz, -40°C ≤T_A ≤ 125°C	70.5	72		dB
THD	Total harmonic distortion	f_{IN}=100kHz, -40°C ≤T_A ≤ 125°C		-82		dB
SFDR	Spurious-free dynamic range	f_{IN}=100kHz, -40°C ≤T_A ≤ 125°C		84		dB
IMD	Intermodulation distortion, third order terms	f_a=108kHz, f_b=109kHz		-80		dB
FPBW	-3dB full power bandwidth	5V supply		10		MHz
		3V supply		7.7		MHz
POWER SUPPLY CHARACTERISTICS						
I_{DD}	Normal mode (static)	V_{DD} = 4.75V to 5.25V, SCLK On or Off		1		mA
		V_{DD} = 2.7V to 3.6V, SCLK On or Off		0.9		mA
	Normal mode (operational)	V_{DD} = 4.75V to 5.25V, f_{SAMPLE} = 1MSPS, -40°C ≤T_A ≤ 125°C		2.2	3.0	mA
		V_{DD} = 2.7V to 3.6V, f_{SAMPLE} = 1MSPS, -40°C ≤T_A ≤ 125°C		1.5	2.0	mA
	Shutdown mode	V_{DD} = 5V, SCLK Off		1		µA
		V_{DD} = 5V, SCLK On		50		µA
P_D	Power consumption, normal mode (operational)	V_{DD} = 5V, f_{SAMPLE} = 1MSPS, -40°C ≤T_A ≤ 125°C		11	15	mW
		V_{DD} = 3V, f_{SAMPLE} = 1MSPS, -40°C ≤T_A ≤ 125°C		4.5	6	mW
	Power consumption, shutdown mode	V_{DD} = 5V, SCLK Off		5		µW
		V_{DD} = 3V, SCLK Off		3		µW
ANALOG INPUT CHARACTERISTICS						
V_{IN}	Input range			0 to V_{DD}		V
I_{DCL}	DC leakage current			±1		µA
C_{INA}	Analog input capacitance			36		pF
DIGITAL INPUT CHARACTERISTICS						
V_{IH}	Input high voltage	-40°C ≤ T_A≤ 125°C	2.4			V
V_{IL}	Input low voltage	V_{DD} = 5V, -40°C ≤T_A ≤ 125°C			0.8	V
		V_{DD} = 3V, -40°C ≤T_A ≤ 125°C			0.4	V

(1) Data sheet minimum and maximum specification limits are ensured by design, test, or statistical analysis.

Electrical Characteristics(continued)

T_A = 25°C, V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, and f_{SAMPLE} = 1 MSPS (unless otherwise noted) (1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
I_{IN}	Input current	V_{IN} = 0V or V_{DD}		±100		nA
C_{IND}	Digital input capacitance			4		pF
DIGITAL OUTPUT CHARACTERISTICS						
V_{OH}	Output high voltage	I_{SOURCE} = 200μA, V_{DD} = 2.7V to 5.25V, -40°C ≤ T_A ≤ 125°C	V_{DD}-0.2			V
V_{OL}	Output low voltage	I_{SINK} = 200μA, -40°C ≤T_A ≤ 125°C			0.4	V
I_{OL}	TRI-STATE leakage current	-40°C ≤T_A ≤ 125°C			±10	μA
C_{OUT}	TRI-STATE output capacitance	-40°C ≤T_A ≤ 125°C		4		pF
	Output Coding		Straight (natural) binary			
AC ELECTRICAL CHARACTERISTICS						
f_{SCLK}	Clock frequency	-40°C ≤T_A ≤ 125°C			20	MHz
DC	SCLK duty cycle	-40°C ≤T_A ≤ 85°C	40%		60%	
t_{TH}	Track or hold acquisition time	-40°C ≤T_A ≤ 85°C			400	ns
f_{RATE}	Throughput rate	-40°C ≤T_A ≤ 85°C			1	MSPS
t_{AD}	Aperture delay			7.5		ns
t_{AJ}	Aperture jitter			30		ps

(1) Data sheet minimum and maximum specification limits are ensured by design, test, or statistical analysis.

7.5 Timing Requirements

-40°C ≤ T_A ≤ 125°C, V_{DD} = 2.7 V to 5.25 V, and f_{SCLK} = 20 MHz (unless otherwise noted) (1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
$t_{CONVERT}$				16×t_{SCLK}		
t_{QUIET}	Quiet time (2)		50			ns
t_1	Minimum CS pulse width		10			ns
t_2	CS to SCLK setup time		10			ns
t_3	Delay from CS until SDATA TRI-STATE disabled (3)				20	ns
t_4	Data access time after SCLK falling edge (4)	V_{DD} = 2.7V to 3.6V			40	ns
		V_{DD} = 4.75V to 5.25V			20	ns
t_5	SCLK low pulse width		0.4×t_{SCLK}			ns
t_6	SCLK high pulse width		0.4×t_{SCLK}			ns
t_7	SCLK to data valid hold time	V_{DD} = 2.7V to 3.6V	7			ns
		V_{DD} = 4.75V to 5.25V	5			ns
t_8	SCLK falling edge to SDATA high impedance (5)	V_{DD} = 2.7V to 3.6V	6		25	ns
		V_{DD} = 4.75V to 5.25V	5		25	ns
$t_{POWER-UP}$	Power-up time from full power down	T_A = 25°C		1		μs

(1) All input signals are specified as t_r = t_f = 5 ns (10% to 90% V_{DD}) and timed from 1.6 V.
(2) Minimum quiet time required between bus relinquish and start of next conversion.
(3) Measured with 25pF load, and defined as the time taken by the output to cross 1 V.
(4) Measured with 25pF load, and defined as the time taken by the output to cross 1 V or 2 V.
(5) t_8 is derived from the time taken by the outputs to change by 0.5 V.

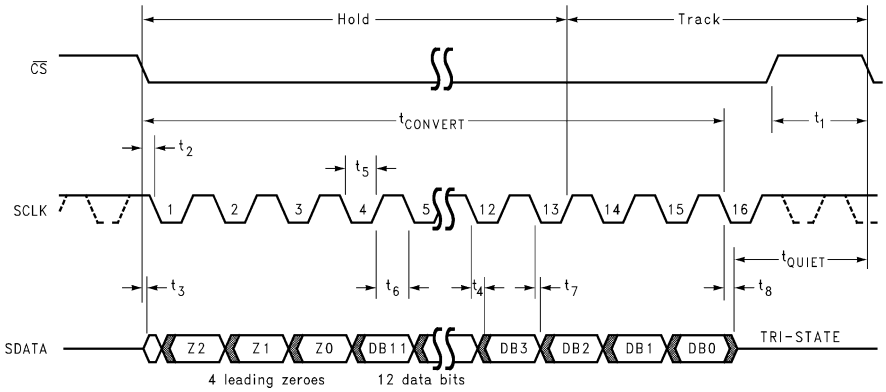


Figure 1. RS1461 Serial Interface Timing Diagram

7.6 TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 20 MHz, and f_{IN} = 100 kHz (unless otherwisenoted).

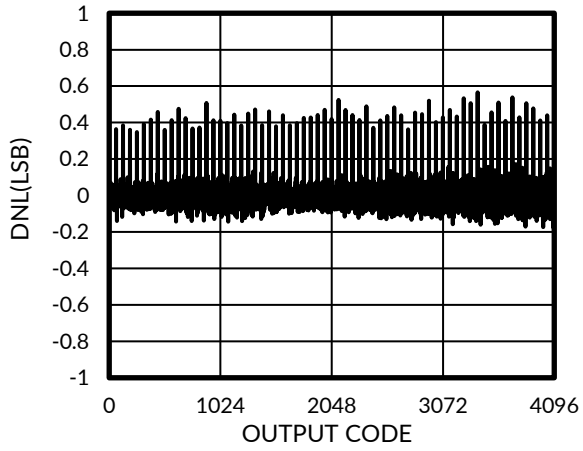


Figure 2. DNL vs OUTPUT CODE

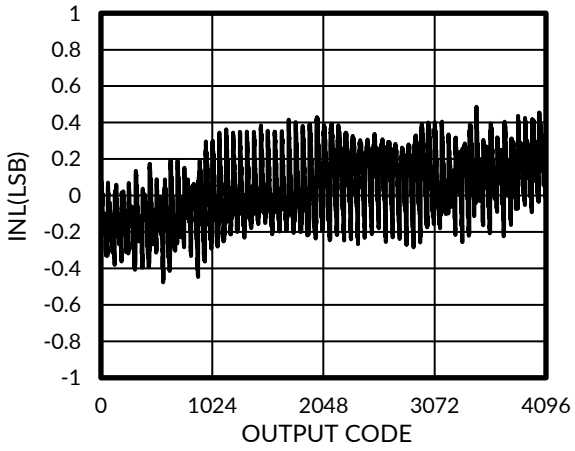


Figure 3. INL vs OUTPUT CODE

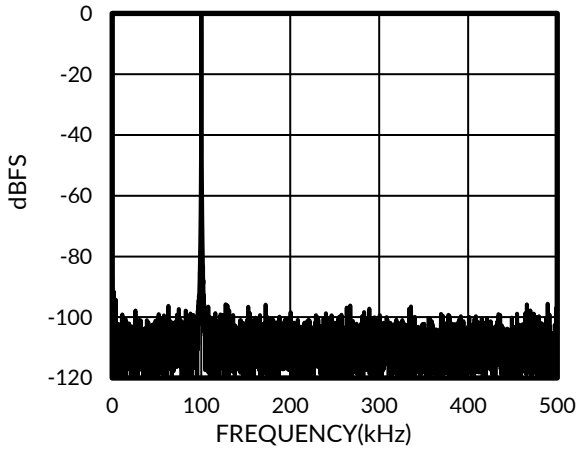


Figure 4. Spectral Response at 100kHz Input

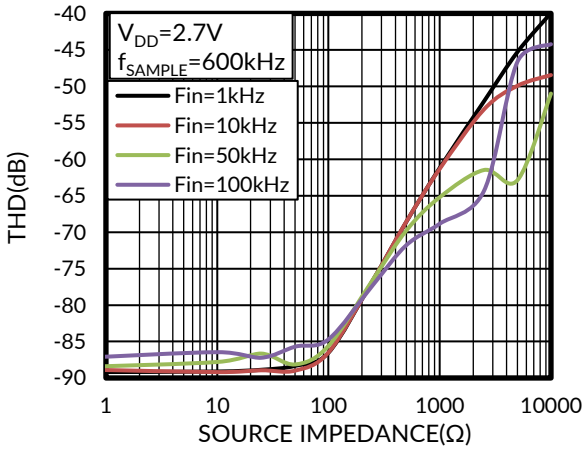


Figure 5. THD vs Source Impedance

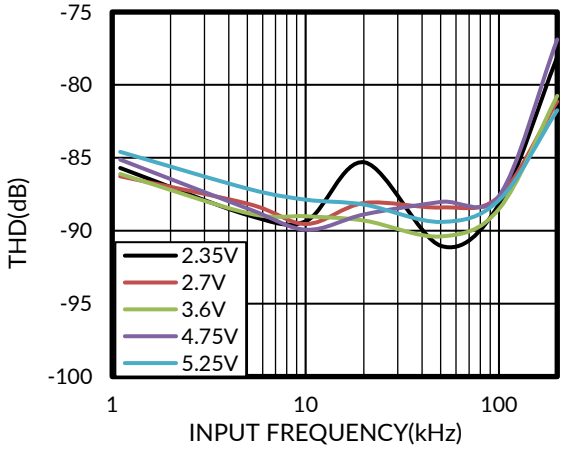


Figure 6. THD vs Input Frequency, 600KSPS

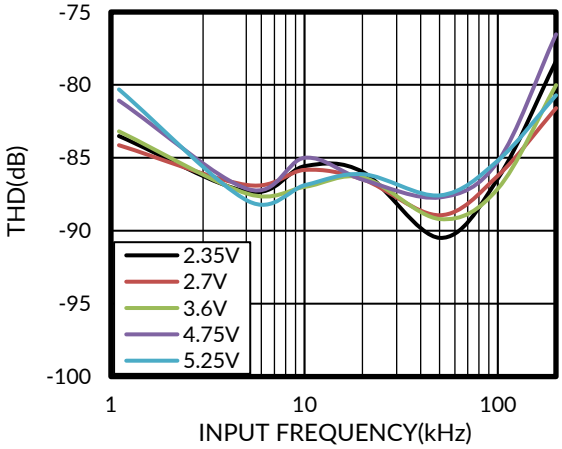


Figure 7. THD vs Input Frequency, 1MSPS

TYPICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 20 MHz, and f_{IN} = 100 kHz (unless otherwisenoted)

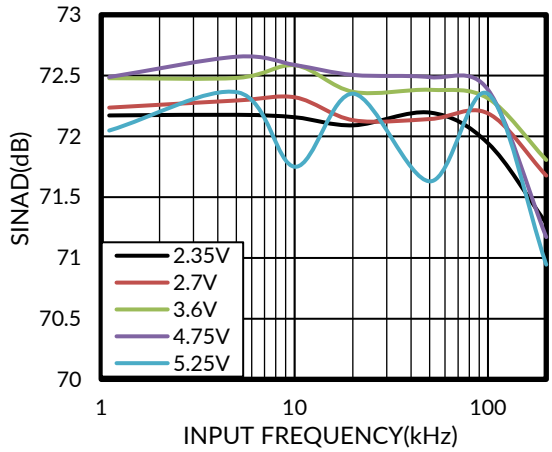


Figure 8. SINAD vs Input Frequency, 600KSPS

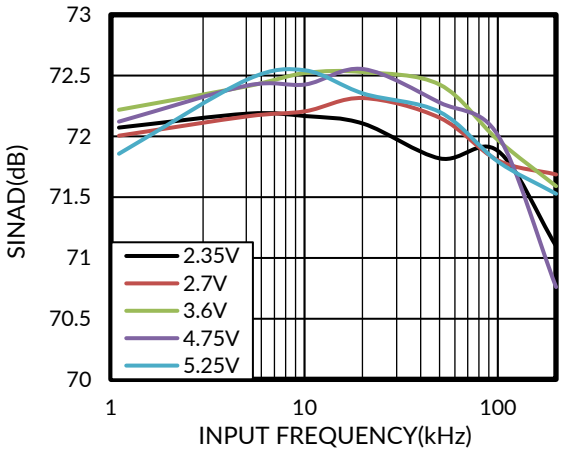


Figure 9. SINAD vs Input Frequency, 1MSPS

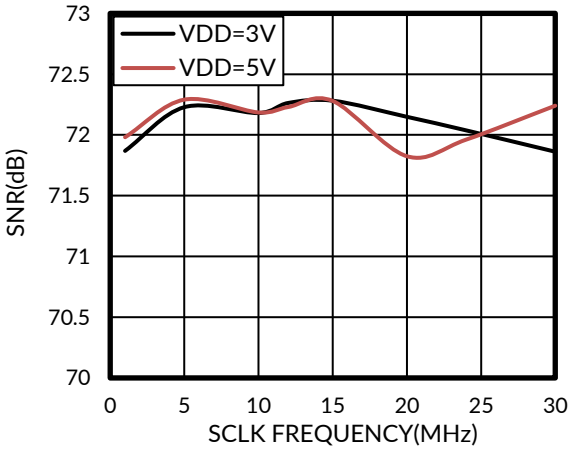


Figure 10. SNR vs F_{SCLK}

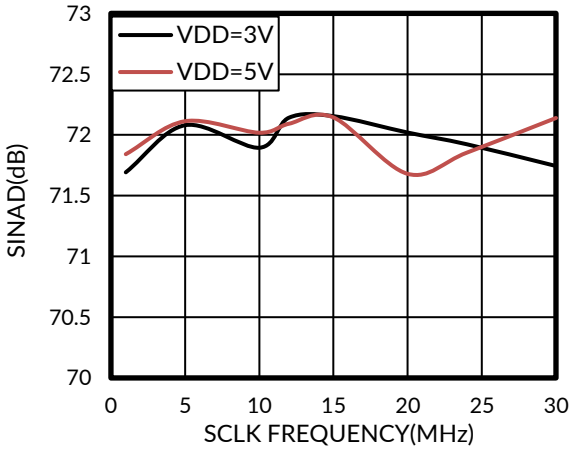


Figure 11. SINAD vs F_{SCLK}

8 DETAILED DESCRIPTION

8.1 Overview

The RS1461 is a successive-approximation analog-to-digital converter designed around a charge-redistribution digital-to-analog converter. Simplified schematics of the RS1461 in both track and hold operation are shown in Figure 13 and Figure 14. In Figure 14, the device is in track mode where the switch SW1 connects the sampling capacitor to the input, and SW2 balances the comparator inputs. The device is in this state until $\overline{CS}$ is brought low, at which point the device moves to hold mode.

8.2 Functional Block Diagram

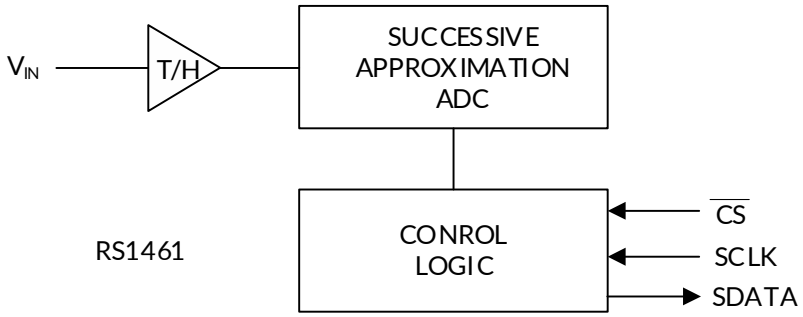


Figure 12. RS1461 Functional Block Diagram

8.3 Feature Description

Serial interface timing diagram for the RS1461 is shown in Figure 1. $\overline{CS}$ is chip select, which initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. SDATA is the serial data out pin, where a conversion result is found.

Basic operation of the RS1461 begins with $\overline{CS}$ going low, which initiates a conversion process and data transfer. Subsequent rising and falling edges of SCLK will be labeled with reference to the falling edge of $\overline{CS}$; for example, the third falling edge of SCLK shall refer to the third falling edge of SCLK after $\overline{CS}$ goes low.

At the fall of $\overline{CS}$, the SDATA pin comes out of TRI-STATE, and the converter moves from track mode to hold mode. The input signal is sampled and held for conversion at the falling edge of $\overline{CS}$. The converter moves from hold mode to track mode on the 13th rising edge of SCLK (see Figure 1). The SDATA pin is placed back into TRI-STATE after the 16th falling edge of SCLK, or at the rising edge of $\overline{CS}$, whichever occurs first. After a conversion is completed, the quiet time t_{QUIET} must be satisfied before bringing $\overline{CS}$ low again to begin another conversion.

Sixteen SCLK cycles are required to read a complete sample from the RS1461. The sample bits (including any leading or trailing zeroes) are clocked out on falling edges of SCLK, and are intended to be clocked in by a receiver on subsequent falling edges of SCLK. RS1461 produces four leading zeroes on SDATA, followed by twelve data bits (the most significant first). The least significant data bit is valid on the 16th falling edge of SCLK.

Depending upon the application, the first edge on SCLK after $\overline{CS}$ goes low may be either a falling edge or a rising edge. If the first SCLK edge after $\overline{CS}$ goes low is a rising edge, all four leading zeroes are valid on the first four falling edges of SCLK. If instead the first SCLK edge after $\overline{CS}$ goes low is a falling edge, the first leading zero may not be set up in time for a microprocessor or DSP to read it correctly. The remaining data bits are still clocked out on the falling edges of SCLK.

8.4 Device Functional Modes

Figure 13 shows the device in hold mode where the switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add or subtract fixed amounts of charge from the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The device moves from hold mode to track mode (Figure 14) on the 13th rising edge of SCLK.

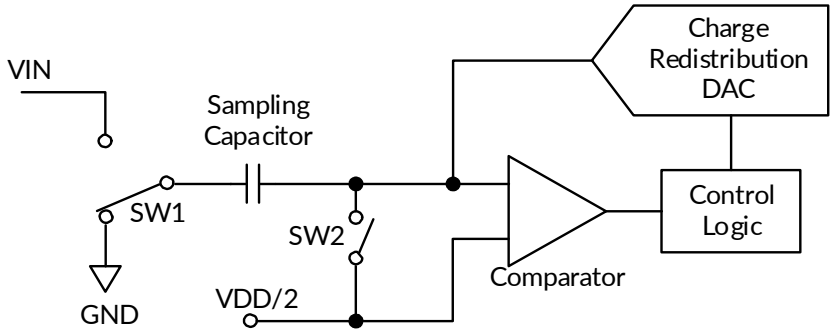


Figure 13. RS1461 in Hold Mode

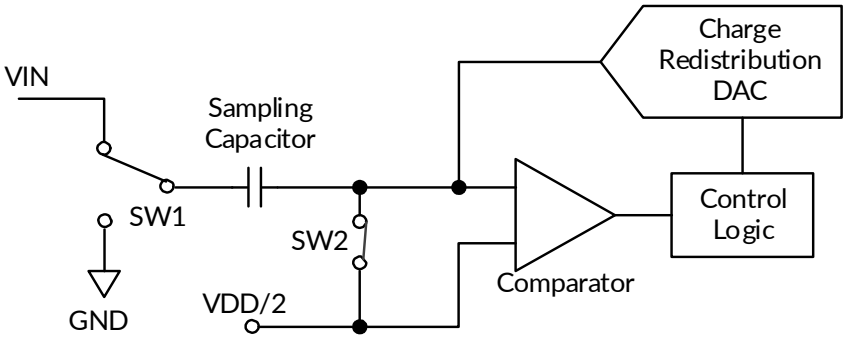


Figure 14. RS1461 in Track Mode

8.4.1 Transfer Function

The output format of RS1461 is straight binary. Code transitions occur midway between successive integer LSB values. The ideal transfer characteristic for the RS1461 is shown in Figure 15.

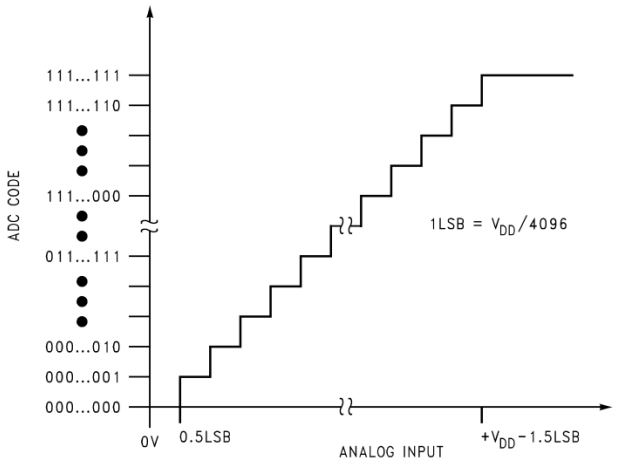


Figure 15. RS1461 Ideal Transfer Characteristic

8.4.2 Power-up Timing

The RS1461 typically requires 1μs to power up, either after first applying V_{DD}, or after returning to normal mode from shutdown mode. This corresponds to one dummy conversion for any SCLK frequency within the specifications in this document. After this first dummy conversion, the RS1461 performs conversions properly.

8.4.3 Modes of Operation

The RS1461 has two possible modes of operation: Normal Mode and Shutdown Mode. ADCS747x enters normal mode (and a conversion process is begun) when $\overline{CS}$ is pulled low. The device enters shutdown mode if $\overline{CS}$ is pulled high before the tenth falling edge of SCLK after $\overline{CS}$ is pulled low, or stays in normal mode if $\overline{CS}$ remains low. Once in shutdown mode, the device stays there until $\overline{CS}$ is brought low again. By varying the ratio of time spent in the normal and shutdown modes, a system may trade off throughput for power consumption.

8.4.3.1 Normal Mode

The best possible throughput is obtained by leaving the RS1461 in normal mode at all times, so there are no power-up delays. To keep the device in normal mode continuously, $\overline{CS}$ must be kept low until after the 10th falling edge of SCLK after the start of a conversion (remember that a conversion is initiated by bringing $\overline{CS}$ low).

If $\overline{CS}$ is brought high after the 10th falling edge, but before the 16th falling edge, the device remains in normal mode, but the current conversion is aborted, and SDATA returns to TRI-STATE (truncating the output word).

Sixteen SCLK cycles are required to read all of a conversion word from the device. After sixteen SCLK cycles have elapsed, $\overline{CS}$ may be idled either high or low until the next conversion. If $\overline{CS}$ is idled low, it must be brought high again before the start of the next conversion, which begins when $\overline{CS}$ is again brought low.

After sixteen SCLK cycles, SDATA returns to TRI-STATE. Another conversion may be started, after t_{QUIET} has elapsed, by bringing $\overline{CS}$ low again.

8.4.3.2 Start-Up Mode

When the V_{DD} supply is first applied, the RS1461 may power up in either of the two modes: normal or shutdown. As such, one dummy conversion should be performed after start-up, exactly as described in Power- Up Timing. The part may then be placed into either normal mode or the shutdown mode, as described in Normal Mode and Shutdown Mode.

8.4.3.3 Shutdown Mode

Shutdown mode is appropriate for applications that either do not sample continuously, or are willing to trade throughput for power consumption. When the RS1461 is in shutdown mode, all of the analog circuitry is turned off.

To enter shutdown mode, a conversion must be interrupted by bringing $\overline{CS}$ back high anytime between the second and tenth falling edges of SCLK, as shown in Figure 16. Once $\overline{CS}$ has been brought high in this manner, the device enters shutdown mode; the current conversion is aborted and SDATA enters TRI-STATE. If $\overline{CS}$ is brought high before the second falling edge of SCLK, the device does not change mode; this is to avoid accidentally changing mode as a result of noise on the $\overline{CS}$ line.

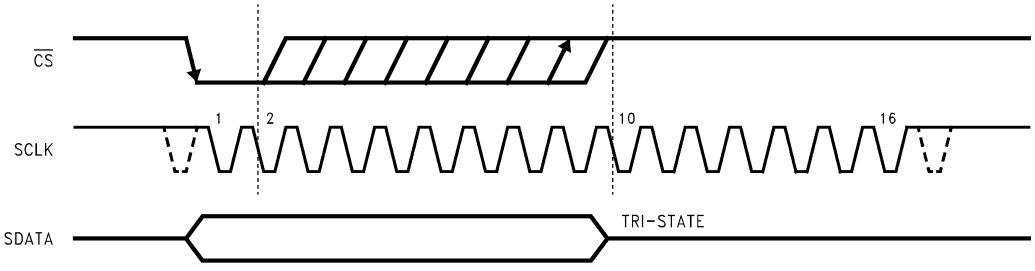


Figure 16. Entering Shutdown Mode

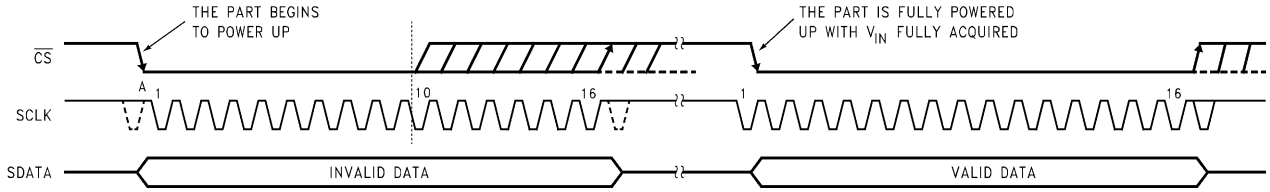


Figure 17. Entering Normal Mode

To exit shutdown mode, bring $\overline{CS}$ back low. Upon bringing $\overline{CS}$ low, the RS1461 begins powering up. Power up typically takes 1μs. This microsecond of power-up delay results in the first conversion result being unusable. The second conversion performed after power-up, however, is valid, as shown in Figure 17.

If $\overline{CS}$ is brought back high before the 10th falling edge of SCLK, the device returns to shutdown mode. This is done to avoid accidentally entering normal mode as a result of noise on the $\overline{CS}$ line. To exit shutdown mode and remain in normal mode, $\overline{CS}$ must be kept low until after the 10th falling edge of SCLK. The RS1461 is fully powered up after 16 SCLK cycles.

9 APPLICATION AND IMPLEMENTATION

9.1 Application Information

A typical application of RS1461 is shown in Figure 18. The combined analog and digital supplies are provided in this example by the low-dropout voltage regulator, available in a variety of fixed and adjustable output voltages. The supply is bypassed with a capacitor network located close to the device. The three-wire interface is also shown connected to a microprocessor or DSP.

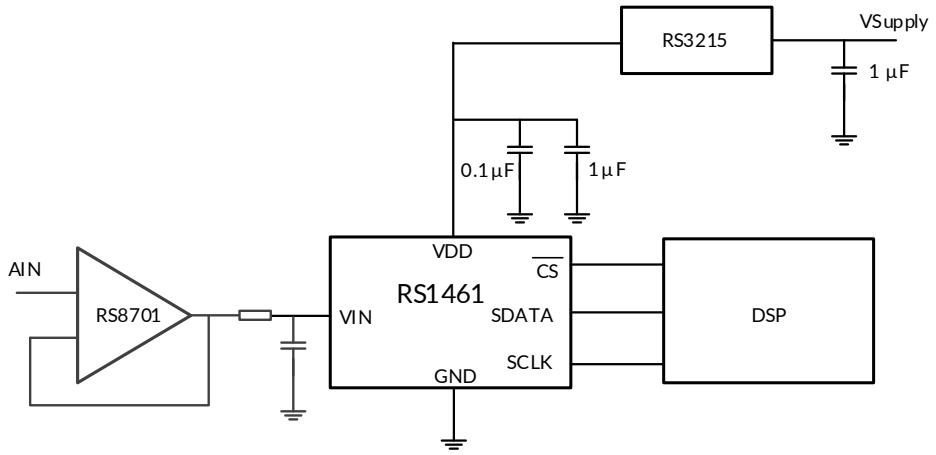


Figure 18. Typical Application Circuit

9.1.1 Analog Input

An equivalent circuit for the RS1461 input channel is shown in Figure 19. The diodes D1 and D2 provide ESD protection for the analog inputs. At no time should an analog input exceed V_{DD} + 300 mV or GND - 300 mV, as these ESD diodes begin conducting current into the substrate or supply line and affect ADC operation.

The capacitor C1 in Figure 19 typically has a value of 4 pF, and is mainly due to pin capacitance. The resistor R1 represents the ON resistance of the multiplexer and track or hold switch, and is typically 100Ω. The capacitor C2 is the RS1461 sampling capacitor, and is typically 32pF.

The sampling nature of the analog input causes input current pulses that result in voltage spikes at the input. RS1461 delivers best performance when driven by a low-impedance source to eliminate distortion caused by the charging of the sampling capacitance. In some applications where dynamic performance is critical, the input must be driven with a low output-impedance amplifier. In addition, when using RS1461 to sample AC signals, a band-pass or low-pass filter reduces harmonics and noise and thus improve THD and SNR.

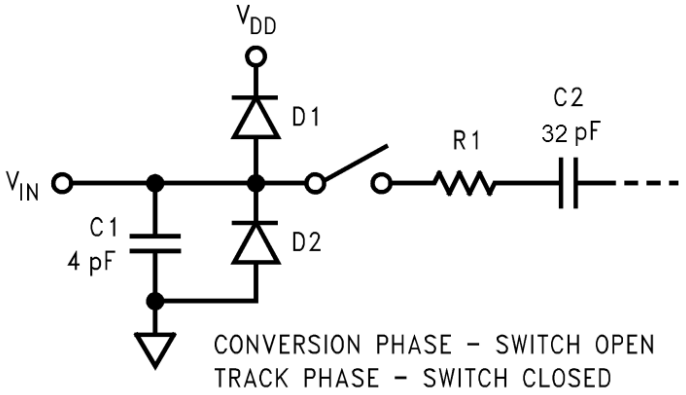


Figure 19. Equivalent Input Circuit

9.1.2 Digital Inputs and Outputs

The RS1461 digital inputs (SCLK and $\overline{CS}$) are not limited by the same absolute maximum ratings as the analog inputs. The digital input pins are instead limited to 5.5V with respect to GND, regardless of V_{DD}, the supply voltage. This allows RS1461 to be interfaced with a wide range of logic levels, independent of the supply voltage.

Note: Even though the digital inputs are tolerant of up to 5.5V above GND, the digital outputs are only capable of driving V_{DD} out.
In addition, the digital input pins are not prone to latch-up; SCLK and $\overline{CS}$ may be asserted before V_{DD} without any risk.

9.2 Power Supply Recommendations

There are three concerns relating to the power supply of these products: the effects of Power Supply Noise upon the conversion process, the Digital Output Effect Upon Noise upon the conversion process, and Power Management of the product.

9.2.1 Power Supply Noise

Because the supply voltage of the RS1461 is the reference voltage, any noise greater than 1/2 LSB in amplitude has some effect upon the converter noise performance. This effect is proportional to the input voltage level. The power supply must receive all the considerations of a reference voltage as far as stability and noise is concerned. Using the same supply voltage for these devices as is used for digital components leads to degraded noise performance.

9.2.2 Digital Output Effect Upon Noise

The charging of any output load capacitance requires current from the digital supply, V_{DD}. The current pulses required from the supply to charge the output capacitance causes voltage variations at the ADC supply line. If these variations are large enough, they could degrade SNR and SINAD performance of the ADC. Similarly, discharging the output capacitance when the digital output goes from a logic high to a logic low dumps current into the die substrate, causing ground bounce noise in the substrate that degrades noise performance if that current is large enough. The larger the output capacitance, the more current flows through the device power supply line and die substrate and the greater is the noise coupled into the analog path.
The first solution to keeping digital noise out of the power supply is to decouple the supply from any other components or use a separate supply for the ADC. To keep noise out of the supply, keep the output load capacitance as small as practical. If the load capacitance is greater than 50 pF, use a 100Ω series resistor at the ADC output, located as close to the ADC output pin as practical. This limits the charge and discharge current of the output capacitance and improve noise performance. Because the series resistor and the load capacitance form a low frequency pole, verify signal integrity when the series resistor is added.

9.2.3 Power Management

When RS1461 is operated continuously in normal mode, throughput up to 1MSPS can be achieved. The user may trade throughput for power consumption by simply performing fewer conversions per unit time and putting the RS1461 into shutdown mode between conversions. This method is not advantageous beyond 350kSPS throughput.
A plot of maximum power consumption versus throughput is shown in Figure 20. To calculate the power consumption for a given throughput, remember that each time the part exits shutdown mode and enters normal mode, one dummy conversion is required. Generally, the user puts the part into normal mode, execute one dummy conversion followed by one valid conversion, and then put the part back into shutdown mode. When this is done, the fraction of time spent in normal mode may be calculated by multiplying the throughput (in samples per second) by 2µs, the time taken to perform one dummy and one valid conversion. The power consumption can then be found by multiplying the fraction of time spent in normal mode by the normal mode power consumption figure. The power dissipated while the part is in shutdown mode is negligible. For example, to calculate the power consumption at 300kSPS with V_{DD} = 5V, begin by calculating the fraction of time spent in normal mode: 300,000 samples/second x 2µs = 0.6, or 60%. The power consumption at 300kSPS is then 60% of 15mW (the maximum power consumption at V_{DD} = 5V) or 9mW.

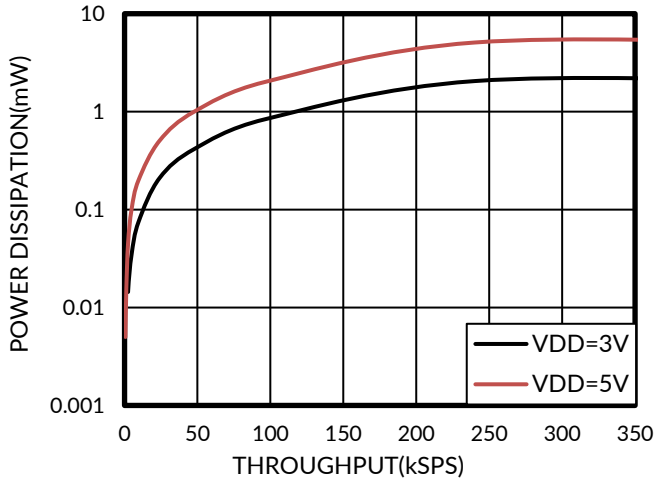
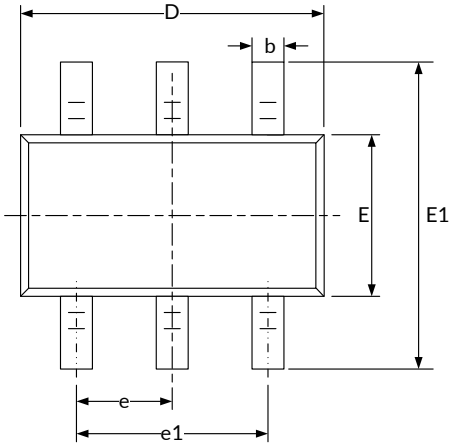
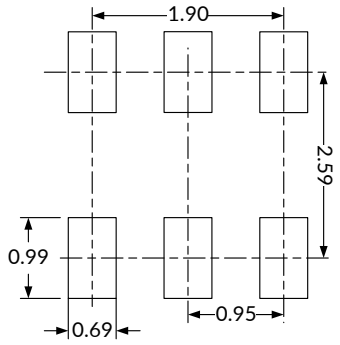


Figure 20. Maximum Power Consumption vs Throughput

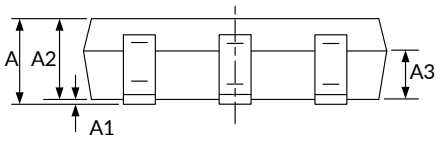
10 PACKAGE OUTLINE DIMENSIONS

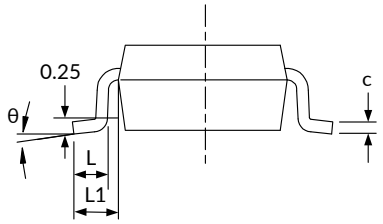
SOT23-6 (4)





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.250		0.049
A1	0.040	0.100	0.001	0.004
A2	1.000	1.200	0.039	0.047
A3	0.600	0.700	0.023	0.028
b	0.380	0.460	0.015	0.018
c	0.130	0.170	0.005	0.007
D (1)	2.820	3.020	0.111	0.119
E (1)	1.500	1.700	0.059	0.067
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC) (2)		0.037 (BSC) (2)	
e1	1.900 (BSC) (2)		0.075 (BSC) (2)	
L	0.300	0.600	0.012	0.024
L1	0.600 (REF) (3)		0.024 (REF) (3)	
θ	0°	8°	0°	8°

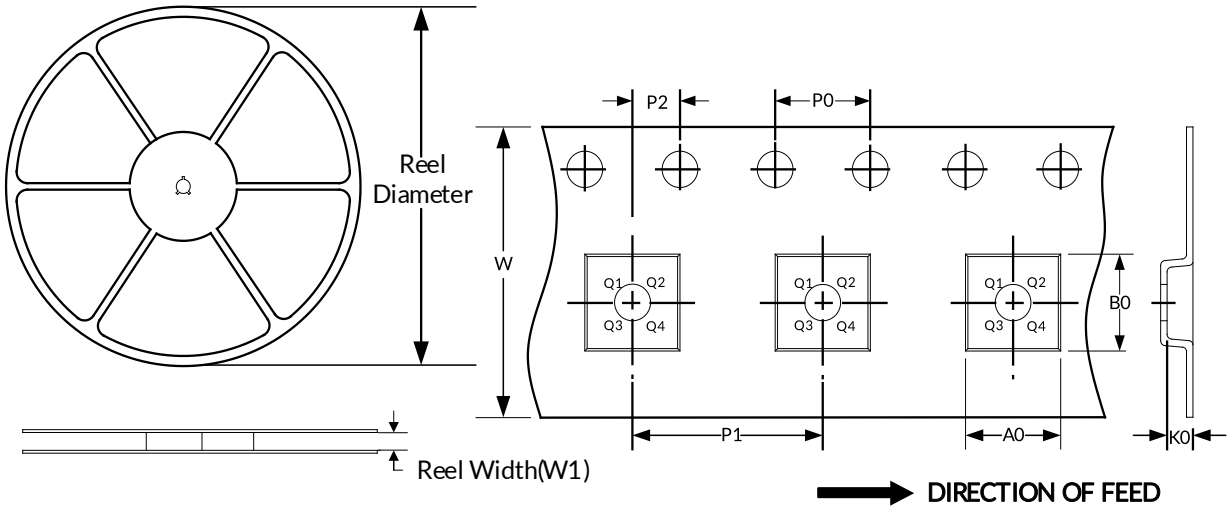
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. REF is the abbreviation for Reference.
4. This drawing is subject to change without notice.

11 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT23-6	7"	9.5	3.17	3.23	1.37	4.0	4.0	2.0	8.0	Q3

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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